

**Amendments to the Claims**

This listing of claims will replace all prior versions, and listing, of claims in the application:

**Listing of Claims:**

1. (Original) A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:
  - growing a thermal layer on a first side of a first silicon wafer;
  - depositing a nitride layer on the thermal layer;
  - depositing, patterning and removing portions of first metal layer on the nitride layer for a plurality of devices;
  - depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;
  - patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a plurality of pump-out ports through the first silicon wafer and layers on the first silicon wafer;
  - masking and removing material from a first side of a second silicon wafer to form a plurality of recesses in the first side of the second silicon wafer;
  - forming a sealing ring on the first side of the second silicon wafer around each of the plurality of recesses; and

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first silicon wafer;

each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second silicon wafers are effectively a bonded together set of wafers.

2. (Original) The method of claim 1, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

3. (Original) The method of claim 2, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

4. (Original) The method of claim 3, further comprising coating the second wafer with antireflection material.

5. (Original) The method of claim 4, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8-14 micron wavelength region of light going through the second silicon wafer to the plurality of devices.

6. (Original) The method of claim 5, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

7. (Original) The method of claim 6, wherein the plurality of devices comprise thermoelectric detectors.

8. (Original) The method of claim 6, wherein the plurality of devices comprise bolometers.

9. (Original) A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first thermal layer on a first side of a first silicon wafer;

depositing a nitride layer on the first thermal layer;

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

depositing and patterning a first metal layer on the nitride layer for at least one device;  
depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a pump-out port through the first silicon wafer and the layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer, to form a recess in the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around the recess; and  
positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

the sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

the at least one device is within the recess resulting in a chamber containing the at least one device;

the pump-out port is within the sealing ring; and

the first and second silicon wafers are effectively a bonded together set of wafers.

10. (Original) The method of claim 9, further comprising:

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the pump-out port on the second side of the first silicon wafer, wherein the chamber is sealed from the environment.

11. (Original) The method of claim 10, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first silicon wafer.

12. (Original) The method of claim 11, wherein the at least one device is a detector.

13. (Original) The method of claim 12, further comprising coating the second silicon wafer with antireflection material.

14. (Original) The method of claim 11, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8-14 micron wavelength region of light going through the second silicon wafer to the at least one device.

15. (Original) The method of claim 14, wherein the at least one device is a thermoelectric detector.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

16. (Original) The method of claim 14, wherein the at least one device is a bolometer.
17. (Original) The method of claim 11, wherein the at least one device is an emitter.
18. (Original) A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:
- growing a first layer of thermal SiO<sub>2</sub> on a first side of a first silicon wafer;
  - depositing a first layer of Si<sub>3</sub> N<sub>4</sub> on the first layer of thermal SiO<sub>2</sub>;
  - growing a second layer of thermal SiO<sub>2</sub> on a second side of the first silicon wafer;
  - depositing a second layer of Si<sub>3</sub> N<sub>4</sub> on the second layer of thermal SiO<sub>2</sub>;
  - depositing a layer of a first metal on the second layer of Si<sub>3</sub> N<sub>4</sub>;
  - patterning the layer of the first metal;
  - depositing a layer of a second metal on the layer of the first metal;
  - patterning the layer of the second metal;
  - depositing a third layer of Si<sub>3</sub> N<sub>4</sub> on the layers of the first and second metals;
  - etching at least one via through the third layer of Si<sub>3</sub> N<sub>4</sub>, the layers of the second and first metals, the second layer of Si<sub>3</sub> N<sub>4</sub> and the second layer of thermal SiO<sub>2</sub>;
  - etching a pump-out port through the first layer of SiO<sub>2</sub> and a first portion of the silicon wafer proximate to the at least one via;

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

etching within the at least one via through a second portion of the silicon wafer to the pump-out port;

growing a third layer of thermal  $\text{SiO}_2$  on a first side of a second silicon wafer and a fourth layer of thermal  $\text{SiO}_2$  on a second side of the second silicon wafer;

growing a fourth layer of  $\text{Si}_3\text{N}_4$  on the third layer of thermal  $\text{SiO}_2$  and a fifth layer of  $\text{Si}_3\text{N}_4$  on the fourth layer of  $\text{SiO}_2$ ;

patternning and cutting the fourth layer  $\text{Si}_3\text{N}_4$  and the third layer of thermal  $\text{SiO}_2$  for a bond pad area;

etching a first portion of the second silicon wafer through the fourth  $\text{Si}_3\text{N}_4$  layer and third  $\text{SiO}_2$  layer for the bond pad area;

patternning and cutting the fifth layer of  $\text{Si}_3\text{N}_4$  and fourth layer of thermal  $\text{SiO}_2$  for a recess area;

etching a second portion from the second side of the second silicon wafer to form a recess;

applying an optical coating to the second silicon wafer to substantially reduce reflections;

applying a solder ring proximate to a perimeter of the recess, on the second side of the second silicon wafer;

aligning the first silicon wafer with the second silicon wafer, having the first side of the first silicon wafer and the second side of the second silicon wafer face each other;

putting the first and second silicon wafers in a vacuum;

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

pressing the first and second silicon wafers together with a pressure;  
ramping the temperature of the silicon wafers up to a high temperature;  
increasing the pressure of the first and second silicon wafers against each other to bond the silicon wafers to each other;  
baking out the first and second silicon wafers;  
cooling down the first and second silicon wafers under a maintained vacuum;  
depositing a layer of a metal on the second side of the second silicon wafer to plug the pump-out port to seal the recess with a vacuum; and  
removing the bonded first and second silicon wafers from the vacuum.

19. (Original) A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:  
growing a thermal layer on a first side of a first silicon wafer;  
patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a plurality of pump-out ports through the first silicon wafer and layers on the first silicon wafer;  
masking and removing material from a first side of a second silicon wafer to form a plurality of recesses in the first side of the second silicon wafer;  
forming a sealing ring on the first side of the second silicon wafer around each of the plurality of recesses; and



Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

each recess of the plurality of recesses results in a chamber;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports;

and

the first and second silicon wafers are effectively a bonded together set of wafers.

20. (Original) The method of claim 19, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

21. (Original) The method of claim 20, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

22. (Original) The method of claim 21, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

23. (Original) The method of claim 22, wherein the one or more sealed chambers contains one or more devices.

24. (Original) The method of claim 19, further comprising:  
placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and  
depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from an ambient environment.

25. (Previously Presented) A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first wafer;  
depositing a nitride layer on the thermal layer;  
depositing, patterning and removing portions of first metal layer on the nitride layer for a plurality of devices;  
depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a plurality of pump-out ports through the first wafer and layers on the first wafer;

masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;

forming a sealing ring on the first side of the second wafer around each of the plurality of recesses; and

positioning the first side of the first wafer next to the first side of the second wafer; and wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first wafer;

each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second wafers are effectively a bonded together set of wafers.

26. (Previously Presented) The method of claim 25, further comprising:  
placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

depositing a layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer, wherein each chamber is sealed from the environment.

27. (Previously Presented) The method of claim 26, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first wafer.

28. (Previously Presented) The method of claim 27, further comprising coating the second wafer with antireflection material.

29. (Previously Presented) The method of claim 28, wherein the second wafer is made from a material that is at least substantially transparent to light in the infrared spectrum.

30. (Previously Presented) The method of claim 29, wherein the plurality of devices comprise thermoelectric detectors.

31. (Previously Presented) The method of claim 30, wherein the plurality of devices comprise bolometers.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

32. (Previously Presented) A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

- growing a first thermal layer on a first side of a first wafer;
- depositing a nitride layer on the first thermal layer;
- depositing and patterning a first metal layer on the nitride layer for at least one device;
- depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;
- patterning and removing material from the first wafer and layers on the first side of the first wafer and from a second side of the first wafer to make a pump-out port through the first wafer and the layers on the first wafer;
- masking and removing material from a first side of a second wafer, to form a recess in the first side of the second wafer;
- forming a sealing ring on the first side of the second wafer around the recess;
- positioning the first side of the first wafer next to the first side of the second wafer; and
- wherein:
  - the sealing ring is in contact with at least one of the layers on the first side of the first wafer;
  - the at least one device is within the recess resulting in a chamber containing the at least one device;
  - the pump-out port is within the sealing ring; and
  - the first and second wafers are effectively a bonded together set of wafers.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

33. (Previously Presented) The method of claim 32, further comprising:  
placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and  
depositing a layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer, wherein the chamber is sealed from the environment.

34. (Previously Presented) The method of claim 33, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first wafer.

35. (Previously Presented) The method of claim 34, wherein the at least one device is a detector.

36. (Previously Presented) The method of claim 35, wherein the at least one device is a thermoelectric detector.

37. (Previously Presented) The method of claim 34, wherein the at least one device is an emitter.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

38. (Previously Presented) A method for making a wafer-pair having sealed chambers, comprising:

- patterning and removing material from a first wafer to make a plurality of pump-out ports through the first wafer;
- masking and removing material from a first side of a second wafer to form a plurality of recesses in the first side of the second wafer;
- forming a sealing ring on a first side of the first wafer or the first side of the second wafer such that the sealing ring extends around each of the plurality of recesses; and
- positioning the first side of the first wafer next to the first side of the second wafer; and

wherein:

- each sealing ring is in contact with the first side of the first wafer and the first side of the second wafer
- each recess of the plurality of recesses results in a chamber;
- each sealing ring encloses at least one pump-out port of the plurality of pump-out ports;

and

the first and second wafers are effectively a bonded together set of wafers.

39. (Previously Presented) The method of claim 38, further comprising:

- placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from the environment.

40. (Previously Presented) The method of claim 39, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer.

41. (Previously Presented) The method of claim 40, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

42. (Previously Presented) The method of claim 40, wherein the one or more sealed chambers contains one or more devices.

43. (Previously Presented) The method of claim 38, further comprising:  
placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and

depositing a layer of material on a second side of the first wafer to seal the plurality of pump-out out ports from the second side of the first wafer, wherein each chamber is sealed from an ambient environment.



Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

44. (Currently Amended) A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer;

forming one or more pump-out ports through the first wafer;

positioning a first side of the first wafer next to a first side of the second wafer ~~with a sealing ring therebetween~~, the first wafer and, the second wafer ~~and the sealing ring~~ forming at least part of a chamber, with the pump-out port of the first wafer in fluid communication with the chamber; and

exposing the chamber to a negative pressure relative to atmosphere while plugging the pump out port to seal the chamber.

45. (Currently Amended) A method according to claim 44 further comprising the step of:

making a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess ~~is in registration with~~ forms part of the chamber.

46. (Previously Presented) A method according to claim 44 further comprising the step of:

providing one or more devices in or on the first side of the first wafer and/or the first side of the second wafer before the positioning step.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

47. (Currently Amended) A method according to claim 46 wherein the one or more devices are in ~~registration with~~ the chamber.

48. (Currently Amended) A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer;  
forming one or more pump-out ports through the first wafer;  
making a recess in a first side of the first wafer and/or a first side of the second wafer;  
positioning the first side of the first wafer next to the first side of the second wafer, the first wafer and the second wafer forming a chamber that is at least partially defined by the recess, with the pump-out port of the first wafer in fluid communication with the chamber; and  
exposing the chamber to a negative pressure relative to atmosphere while plugging the  
pump out port to seal the chamber.

49. (Currently Amended) A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer having a first side, with one or more bond pads on the first side;  
providing a second wafer;  
forming one or more bond-pad holes through the second wafer;  
positioning the first side of the first wafer next to a first side of the second wafer ~~with a sealing ring therebetween~~; the first wafer and, the second wafer ~~and the sealing ring~~ forming at

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

least part of a chamber, the first wafer and second wafer being aligned so that the bond-pad holes ~~in the second wafer are in registration with~~ provide physical access to the one or more bond pads on the first wafer through at least selected bond-pad holes in the second wafer; and  
the first and second wafers are effectively a bonded together set of wafers.

50. (Currently Amended) A bonded wafer pair, comprising:  
a first wafer;  
a second wafer;  
the first wafer having one or more pump-out ports through the first wafer;  
the first side of the first wafer bonded to a first side of the second wafer via a sealing ring; the first wafer, the second wafer and the sealing ring forming a chamber, with the pump-out port of the first wafer in fluid communication with the chamber, the chamber having a negative pressure therein relative to atmosphere; and  
a plug for plugging the pump out port.

51. (Currently Amended) A bonded wafer pair according to claim 50 further comprising a recess in the first side of the first wafer and/or the first side of the second wafer, wherein the recess ~~is in registration with~~ forms at least part of the chamber.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

52. (Previously Presented) A bonded wafer pair according to claim 50 further comprising one or more devices in or on the first side of the first wafer and/or the first side of the second wafer.

53. (Currently Amended) A bonded wafer pair according to claim 52 wherein the one or more devices are in ~~registration with~~ the chamber.

54. (Currently Amended) A bonded wafer pair having a sealed chamber, comprising:  
a first wafer;  
a second wafer bonded to the first wafer;  
one or more pump-out ports through the first wafer;  
a recess in a first side of the first wafer and/or a first side of the second wafer;  
the first wafer and the second wafer forming a chamber that includes the recess, with the pump-out port of the first wafer in fluid communication with the chamber, the chamber having a negative pressure therein relative to atmosphere; and  
one or more plugs for plugging the one or more pump out ports to seal the chamber.

55. (Currently Amended) A bonded wafer pair, comprising:  
a first wafer having a first side, with one or more bond pads on the first side;  
a second wafer, with one or more bond-pad holes through the second wafer;

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

the first side of the first wafer bonded to a first side of the second wafer with a sealing ring therebetween, the first wafer and second wafer being aligned so that the bond-pad holes in the second wafer ~~are in registration with~~ provide physical access to the one or more bond pads on the first wafer through at least selected bond-pad holes in the second wafer; and  
the first wafer, the second wafer and the sealing ring forming a chamber.

56. (New) A method according to claim 44 wherein a sealing ring is positioned between the first side of the first wafer and the first side of the second wafer, and wherein the first wafer, the second wafer and the sealing ring form the chamber.

57. (New) A method according to claim 46 wherein the one or more devices include an array of infrared detectors.

58. (New) A bonded wafer pair according to claim 52 wherein the one or more devices include an array of infrared detectors.

59. (New) A method for making a wafer-pair with a sealed chamber therebetween, comprising:

providing a first wafer and a second wafer, the first wafer having a first side and a second side;

forming one or more pump-out ports through the first wafer;

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

positioning the first side of the first wafer next to a first side of the second wafer, the first wafer and the second wafer forming at least part of a chamber, with the pump-out port of the first wafer in fluid communication with the chamber; and

providing one or more layer(s) by deposition to a second side of the first wafer, wherein the one or more deposited layer(s) plug the pump out port and seal the chamber.

60. (New) A method according to claim 59 wherein the one or more layer(s) are deposited by evaporation.

61. (New) A method according to claim 59 wherein the one or more layer(s) are deposited by sputtering.

62. (New) A method according to claim 59 wherein the one or more layer(s) include a metal layer.

63. (New) A method according to claim 59 wherein the one or more layer(s) are deposited in a negative pressure relative to atmosphere.

64. (New) A method according to claim 63 wherein the one or more layer(s) are deposited in a high vacuum environment.

Application No. 10/007,288  
Response dated February 13, 2004  
Reply to Notice of Non-Compliant Amendment dated January 26, 2004

65. (New) An apparatus having a sealed chamber with one or more devices positioned in the sealed chamber, the one or more devices having a desired operating temperature range, the bonded wafer pair comprising:

a first wafer;

a second wafer secured relative to the first wafer;

the first wafer and the second wafer forming a chamber that has a volume, wherein the one or more devices are positioned in the chamber;

one or more pump-out ports through the first wafer, at least one of the one or more pump-out ports in fluid communication with the chamber;

one or more plugs for plugging the one or more pump out ports to seal the chamber; and

the volume of the chamber remaining relatively constant over the desired operating temperature range of the one or more devices.